AMENDMENT

In The Claims:

Claims 1-12 (canceled)

Claim 13 (previously presented) A trench capacitor, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between a surface of said trench and said conducting layer;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate;

a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, wherein said conducting layer, said protruding electrode, and said conducting structure serve as an upper electrode.

Claim 14 (original) The trench capacitor of claim 13, wherein said protruding electrode extends to cover said conducting layer.

Claim 15 (original) The trench capacitor of claim 13, wherein said first and second capacitor dielectric layers are at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer, and a Si3N4/SiO2 (NO) stacked layer.

Claim 16 (original) The trench capacitor of claim 13, wherein said conducting layer and said protruding electrode include doped polysilicon.

Claim 17 (original) The trench capacitor of claim 13, wherein said conducting structure is copper (Cu) or tungsten (W).

Claim 18-24 (canceled)

Claim 25 (previously presented) A dynamic random access memory cell, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between the surface of said trench and said conducting layer;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate;

a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode;

a gate electrode on said substrate beside said protruding electrode;

a plurality of drain/source regions in said substrate beside two sides of said gate electrode;

a gate dielectric layer between said gate electrode and said substrate; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, and said conducting layer, said protruding electrode, and said conducting structure being an upper electrode.

Claim 26 (original) The dynamic random access memory cell of claim 25, wherein said protruding electrode extends to cover said conducting layer.

Claim 27 (original) The dynamic random access memory cell of claim 25, wherein said first and second capacitor dielectric layers is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer and a Si3N4/SiO2 (NO) stacked layer.

Claim 28 (original) The dynamic random access memory cell of claim 25, wherein said conducting layer and said protruding electrode include doped polysilicon.

Claim 29 (original) The dynamic random access memory cell of claim 25, wherein said conducting structure is copper (Cu) -or tungsten (W).

Claim 30 (original) The dynamic random access memory cell of claim 25 further comprising a plurality of spacers on sidewalls of said conducting layer and said gate electrode.

Claim 31 (original) The dynamic random access memory cell of claim 30 further comprising a self-aligned silicide layer on surfaces of said conducting layer and said gate electrode.

Claim 32 (original) The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is the same as a material of said gate dielectric layer.

Claim 33 (original) The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is different from a material of said gate dielectric layer.